2 Megabit (256K x 8) Multi-Purpose Flash
SST39SF020

Preliminary Specifications

FEATURES:

- **Organized as 256 K X 8**
- **Single 5.0V Read and Write Operations**
- **Superior Reliability**
  - Endurance: 100,000 Cycles (typical)
  - Greater than 100 years Data Retention
- **Low Power Consumption:**
  - Active Current: 20 mA (typical)
  - Standby Current: 10 µA (typical)
- **Sector Erase Capability**
  - Uniform 4 KByte sectors
- **Fast Read Access Time:**
  - 70 and 90 ns
- **Latched Address and Data**
- **Fast Sector Erase and Byte Program:**
  - Sector Erase Time: 7 ms (typical)
  - Chip Erase Time: 15 ms (typical)
  - Byte Program time: 20 µs (typical)
  - Chip Rewrite Time: 5 seconds (typical)
- **Automatic Write Timing**
  - Internal V_{pp} Generation
- **End of Write Detection**
  - Toggle Bit
  - Data# Polling
- **TTL I/O Compatibility**
- **JEDEC Standard**
  - EEPROM Pinouts and command set
- **Packages Available**
  - 32-Pin PDIP
  - 32-Pin PLCC
  - 32-Pin TSOP (8mm x 14mm)

PRODUCT DESCRIPTION

The SST39SF020 is a 256K x 8 CMOS Multi-Purpose Flash (MPF) manufactured with SST's proprietary, high performance CMOS SuperFlash technology. The split gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST39SF020 device writes (Program or Erase) with a 5.0V-only power supply. The SST39SF020 device conforms to JEDEC standard pinouts for x8 memories.

Featuring high performance byte program, the SST39SF020 device provides a maximum byte-program time of 30 µsec. The entire memory can be erased and programmed byte by byte typically in 5 seconds, when using interface features such as Toggle Bit or Data# Polling to indicate the completion of Program operation. To protect against inadvertent write, the SST39SF020 device has on-chip hardware and software data protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, the SST39SF020 device is offered with a guaranteed endurance of 10,000 cycles. Data retention is rated at greater than 100 years.

The SST39SF020 device is suited for applications that require convenient and economical updating of program, configuration, or data memory. For all system applications, the SST39SF020 device significantly improves performance and reliability, while lowering power consumption. The SST39SF020 inherently uses less energy during erase and program than alternative flash technologies. The total energy consumed is a function of the applied voltage, current, and time of application. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash technologies. The SST39SF020 device also improves flexibility while lowering the cost for program, data, and configuration storage applications.

The SuperFlash technology provides fixed Erase and Program times, independent of the number of endurance cycles that have occurred. Therefore the system software or hardware does not have to be modified or derated as is necessary with alternative flash technologies, whose erase and program times increase with accumulated endurance cycles.

To meet high density, surface mount requirements, the SST39SF020 device is offered in 32-pin TSOP and 32-pin PLCC packages. A 600 mil, 32-pin PDIP is also available. See Figures 1 and 2 for pinouts.

Device Operation

Commands are used to initiate the memory operation functions of the device. Commands are written to the device using standard microprocessor write sequences. A command is written by asserting WE# low while

keeping CE# low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first.

Read

The Read operation of the SST39SF020 device is controlled by CE# and OE#, both have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to the Read cycle timing diagram for further details (Figure 3).

Byte Program Operation

The SST39SF020 device is programmed on a byte-by-byte basis. The Program operation consists of three steps. The first step is the three-byte-load sequence for Software Data Protection. The second step is to load byte address and byte data. During the Byte Program operation, the addresses are latched on the falling edge of either CE# or WE#, whichever occurs last. The data is latched on the rising edge of either CE# or WE#, whichever occurs first. The third step is the internal Program operation which is initiated after the rising edge of the fourth WE# or CE#, whichever occurs first. The Program operation, once initiated, will be completed, within 30 µs. See Figures 4 and 5 for WE# and CE# controlled Program operation timing diagrams and Figure 14 for flowcharts. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands written during the internal Program operation will be ignored.

Sector Erase Operation

The Sector Erase operation allows the system to erase the device on a sector by sector basis. The sector architecture is based on uniform sector size of 4 KByte. The Sector Erase operation is initiated by executing a six-byte-command load sequence for software data protection with sector erase command (30H) and sector address (SA) in the last bus cycle. The address lines A12-A17 will be used to determine the sector address. The sector address is latched on the falling edge of the sixth WE# pulse , while the command (30H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. The end of Erase can be determined using either Data# Polling or Toggle Bit methods. See Figure 8 for timing waveforms. Any commands written during the Sector Erase operation will be ignored.

Chip-Erase Operation

The SST39SF020 device provides a Chip-Erase operation, which allows the user to erase the entire memory array to the “1’s” state. This is useful when the entire device must be quickly erased.

The Chip Erase operation is initiated by executing a six-byte software data protection command sequence with Chip Erase command (10H) with address 5555H in the last byte sequence. The Erase operation begins with the rising edge of the sixth WE# or CE#, whichever occurs first. During the Erase operation, the only valid read is Toggle Bit or Data# Polling. See Table 4 for the command sequence, Figure 9 for timing diagram, and Figure 17 for the flowchart. Any commands written during the Chip Erase operation will be ignored.

Write Operation Status Detection

The SST39SF020 device provides two software means to detect the completion of a Write (Program or Erase) cycle, in order to optimize the system write cycle time. The software detection includes two status bits : Data# Polling (DQ_7) and Toggle Bit (DQ_6). The end of write detection mode is enabled after the rising edge of WE# which initiates the internal program or erase cycle.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ_7 or DQ_6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

Data# Polling (DQ_7)

When the SST39SF020 device is in the internal Program operation, any attempt to read DQ_7 will produce the complement of the true data. Once the Program operation is completed, DQ_7 will produce true data. The device is then ready for the next operation. During internal Erase operation, any attempt to read DQ7 will produce a ‘0’. Once the internal Erase operation is completed, DQ7 will produce a ‘1’. The Data# Polling is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For sector or chip erase, the Data# Polling is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 6 for Data# Polling timing diagram and Figure 15 for a flowchart.

Toggle Bit (DQ_6)

During the internal Program or Erase operation, any consecutive attempts to read DQ_6 will produce alternating 0's and 1's, i.e., toggling between 0 and 1. The Toggle Bit will begin with "1". When the internal Program or Erase operation is completed, the toggling will stop. The device is then ready for the next operation. The Toggle Bit is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector or Chip Erase, the Toggle Bit is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 7 for Toggle Bit timing diagram and Figure 15 for a flowchart.

Data Protection

The SST39SF020 device provides both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# or CE# pulse of less than 5 ns will not initiate a write cycle.

V_{CC} Power Up/Down Detection: The write operation is inhibited when V_{CC} is less than 2.5V.

Write Inhibit Mode: Forcing OE# low, CE# high, or WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

Software Data Protection (SDP)

The SST39SF020 provides the JEDEC approved software data protection scheme for all data alteration operations, i.e., Program and Erase. Any Program operation requires the inclusion of a series of three byte sequence. The three byte-load sequence is used to initiate the Program operation, providing optimal protection from inadvertent write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of six byte load sequence. The SST39SF020 device is shipped with the software data protection permanently enabled. See Table 4 for the specific software command codes. During SDP command sequence, invalid commands will abort the device to read mode, within TRC.

Product Identification

The product identification mode identifies the device as the SST39SF020 and manufacturer as SST. This mode may be accessed by hardware or software operations. The hardware operation is typically used by a programmer to identify the correct algorithm for the SST39SF020 device. Users may wish to use the software product identification operation to identify the part (i.e., using the device code) when using multiple manufacturers in the same socket. For details, see Table 3 for hardware operation or Table 4 for software operation, Figure 10 for the software ID entry and read timing diagram and Figure 16 for the ID entry command sequence flowchart.

TABLE 1: PRODUCT IDENTIFICATION TABLE

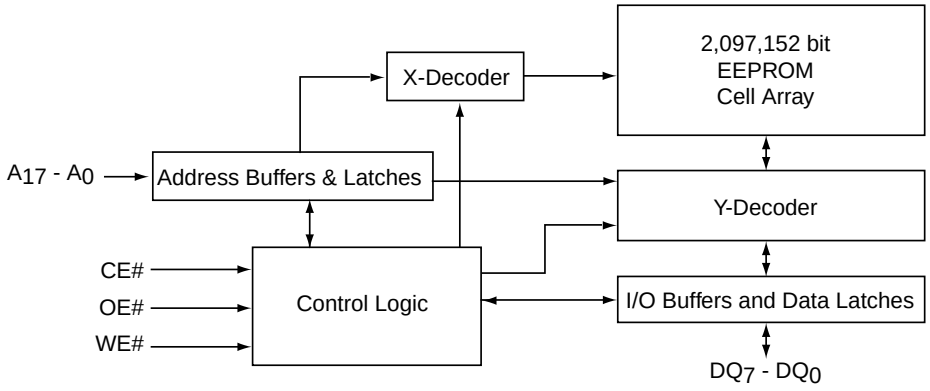
	Address	Data
Manufacturer's Code	0000H	BF H
Device Code	0001H	B6 H

326 PGM T1.2

Product Identification Mode Exit/Reset

In order to return to the standard read mode, the Software Product Identification mode must be exited. Exiting is accomplished by issuing the Exit ID command sequence, which returns the device to the Read operation. Please note that the software reset command is ignored during an internal Program or Erase operation. See Table 4 for software command codes, Figure 11 for timing waveform and Figure 16 for a flowchart.

FUNCTIONAL BLOCK DIAGRAM OF SST39SF020



326 ILL B1.3

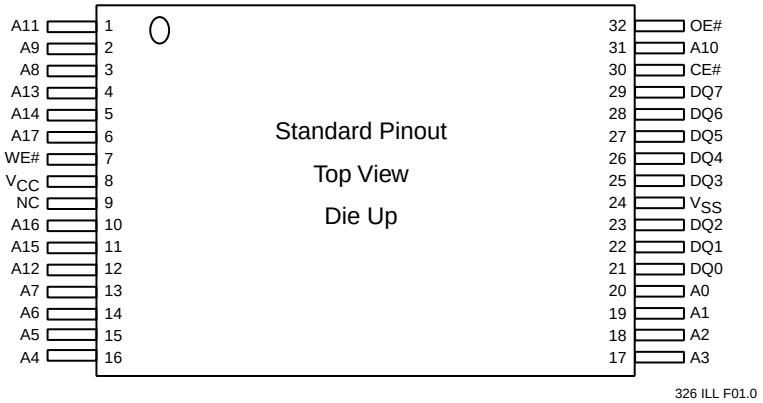


FIGURE 1: PIN ASSIGNMENTS FOR 32-PIN TSOP PACKAGES (8mm x 14mm)

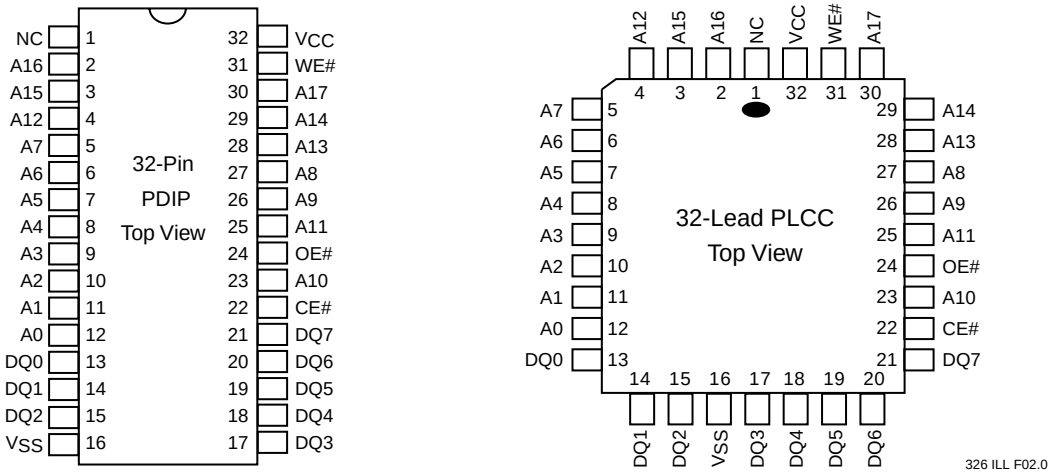


FIGURE 2: PIN ASSIGNMENTS FOR 32-PIN PDIPS AND 32-LEAD PLCCS

Preliminary Specifications

TABLE 2: PIN DESCRIPTION

Symbol	Pin Name	Functions
A_{17}-A_0	Address Inputs	To provide memory addresses. During sector erase A_{17}-A_{12} address lines will select the sector.
DQ_7-DQ_0	Data Input/output	To output data during read cycles and receive input data during write cycles. Data is internally latched during a write cycle. The outputs are in tri-state when OE# or CE# is high.
CE#	Chip Enable	To activate the device when CE# is low.
OE#	Output Enable	To gate the data output buffers.
WE#	Write Enable	To control the write operations.
Vcc	Power Supply	To provide 5-volt supply (± 10%)
Vss	Ground	
NC	No Connection	Unconnected pins.

326 PGM T2.1

TABLE 3: OPERATION MODES SELECTION

Mode	CE#	OE#	WE#	A9	DQ	Address
Read	V_{IL}	V_{IL}	V_{IH}	A_{IN}	D_{OUT}	A_{IN}
Program	V_{IL}	V_{IH}	V_{IL}	A_{IN}	D_{IN}	A_{IN}
Erase	V_{IL}	V_{IH}	V_{IL}	X	X	Sector address, XXh for chip erase
Standby	V_{IH}	X	X	X	High Z	X
Write Inhibit	X	V_{IL}	X	X	High Z/D_{OUT}	X
	X	X	V_{IH}	X	High Z/D_{OUT}	X
Product Identification						
Hardware Mode	V_{IL}	V_{IL}	V_{IH}	V_H	Manufacturer Code (BF) Device Code (B6)	A_{17} - A_1 = V_{IL}, A_0 = V_{IL} A_{17} - A_1 = V_{IL}, A_0 = V_{IH}
Software Mode	V_{IL}	V_{IL}	V_{IH}	A_{IN}	ID Code	See Table 4

326 PGM T3.4

TABLE 4: SOFTWARE COMMAND SEQUENCE

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data
Byte Program	5555H	AAH	2AAAH	55H	5555H	A0H	BA[3]	Data				
Sector Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA_x[2]	30H
Chip Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Software ID Entry	5555H	AAH	2AAAH	55H	5555H	90H						
Software ID Exit	XXH	F0H										
Software ID Exit	5555H	AAH	2AAAH	55H	5555H	F0H						

326 PGM T4.0

Notes:

(1) Address format A_{14}-A_0 (Hex), Addresses A_{15}, A_{16} and A_{17} are a “Don’t Care” for the Command sequence.

(2) SA_x for sector erase; uses A_{17}-A_{12} address lines

(3) BA = Program Byte address

(4) Both Software ID Exit operations are equivalent

Notes for Software ID Entry Command Sequence

1. With A_{17} -A_1 =0; SST Manufacturer Code = BFH, is read with A_0 = 0,
   SST39SF020 Device Code = B6H, is read with A_0 = 1.
2. The device does not remain in Software Product ID Mode if powered down.

Preliminary Specifications

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential ..... -0.5V to V_{CC}+ 0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential ..... -1.0V to V_{CC}+ 1.0V
Voltage on A_9 Pin to Ground Potential ..... -0.5V to 14.0V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Through Hole Lead Soldering Temperature (10 Seconds) ..... 300°C
Surface Mount Lead Soldering Temperature (3 Seconds) ..... 240°C
Output Short Circuit Current(1) ..... 100 mA

Note: (1) Outputs shorted for no more than one second. No more than one output shorted at a time.

OPERATING RANGE

Range	Ambient Temp	V_{CC}
Commercial	0 °C to +70 °C	5V±10%
Industrial	-40 °C to +85 °C	5V±10%

AC CONDITIONS OF TEST

Input Rise/Fall Time ..... 10 ns
Output Load ..... C_L = 100 pF for 90 ns
Output Load ..... C_L = 30 pF for 70 ns
See Figures 12 and 13

TABLE 5: DC OPERATING CHARACTERISTICS V_{CC} = 5V±10%

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{CC}	Power Supply Current Read		30	mA	CE#=OE#=V_{IL},WE#=V_{IH} , all I/Os open, Address input = V_{IL}/V_{IH}, at f=1/T_{RC} Min., V_{CC}=V_{CC} Max
	Write		50	mA	CE#=WE#=V_{IL}, OE#=V_{IH}, V_{CC} =V_{CC} Max.
I_{SB1} (TTL input)	Standby V_{CC} Current		3	mA	CE#=V_{IH}, V_{CC} =V_{CC} Max.
I_{SB2}	Standby V_{CC} Current (CMOS input)		50	µA	CE#=V_{CC} -0.3V. V_{CC} = V_{CC} Max.
I_{LI}	Input Leakage Current		1	µA	V_{IN} =GND to V_{CC}, V_{CC} = V_{CC} Max.
I_{LO}	Output Leakage Current		1	µA	V_{OUT} =GND to V_{CC}, V_{CC} = V_{CC} Max.
V_{IL}	Input Low Voltage		0.8	V	V_{CC} = V_{CC} Max.
V_{IH}	Input High Voltage	2.0		V	V_{CC} = V_{CC} Max.
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.1 mA, V_{CC} = V_{CC} Min.
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400µA, V_{CC} = V_{CC} Min.
V_H	Supervoltage for A_9 pin	11.4	12.6	V	CE# = OE# =V_{IL}, WE# = V_{IH}
I_H	Supervoltage Current for A_9 pin		200	µA	CE# = OE# = V_{IL}, WE# = V_{IH}, A_9 = V_H Max.

326 PGM T5.2

TABLE 6: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$(1)	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$(1)	Power-up to Write Operation	100	µs

326 PGM T6.1

TABLE 7: CAPACITANCE (Ta = 25 °C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$(1)	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pF
C_{IN}(1)	Input Capacitance	V_{IN} = 0V	6 pF

326 PGM T7.0

Note: (1)This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 8: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}(1)	Endurance	10,000	Cycles	MIL-STD-883, Method 1033
T_{DR}(1)	Data Retention	100	Years	JEDEC Standard A103
V_{ZAP_HBM}(1)	ESD Susceptibility Human Body Model	1000	Volts	JEDEC Standard A114
V_{ZAP_MM}(1)	ESD Susceptibility Machine Model	200	Volts	JEDEC Standard A115
I_{LTH}(1)	Latch Up	100 + I_{CC}	mA	JEDEC Standard 78

326 PGM T8.3

Note: (1)This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

AC CHARACTERISTICS

TABLE 9: READ CYCLE TIMING PARAMETERS V_{CC} = 4.5-5.5V

		SST39SF020-70		SST39SF020-90		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
T_{RC}	Read Cycle time	70		90		ns
T_{CE}	Chip Enable Access Time		70		90	ns
T_{AA}	Address Access Time		70		90	ns
T_{OE}	Output Enable Access Time		35		45	ns
T_{CLZ}(1)	CE# Low to Active Output	0		0		ns
T_{OLZ}(1)	OE# Low to Active Output	0		0		ns
T_{CHZ}(1)	CE# High to High-Z Output		15		20	ns
T_{OHZ}(1)	OE# High to High-Z Output		15		20	ns
T_{OH}(1)	Output Hold from Address Change	0		0		ns

326 PGM T9.2

Note: C_L = 100 pF for 90 ns, C_L = 30 pF for 70 ns

TABLE 10: PROGRAM/ERASE CYCLE TIMING PARAMETERS

Symbol	**Parameter**	**Min**	**Max**	**Units**
T_{BP}	Byte Program time		30	µs
T_{AS}	Address Setup Time	0		ns
T_{AH}	Address Hold Time	30		ns
T_{CS}	WE# and CE# Setup Time	0		ns
T_{CH}	WE# and CE# Hold Time	0		ns
T_{OES}	OE# High Setup Time	0		ns
T_{OEH}	OE# High Hold Time	0		ns
T_{CP}	CE# Pulse Width	40		ns
T_{WP}	WE# Pulse Width	40		ns
T_{WPH} (1)	WE# Pulse Width High	30		ns
T_{CPH} (1)	CE# Pulse Width High	30		ns
T_{DS}	Data Setup Time	30		ns
T_{DH} (1)	Data Hold Time	0		ns
T_{IDA} (1)	Software ID Access and Exit Time		150	ns
T_{SE}	Sector Erase		10	ms
T_{SCE}	Chip Erase		20	ms

326 PGM T10.4

Note: (1)This parameter is measured only for initial qualification and after the design or process change that could affect this parameter.

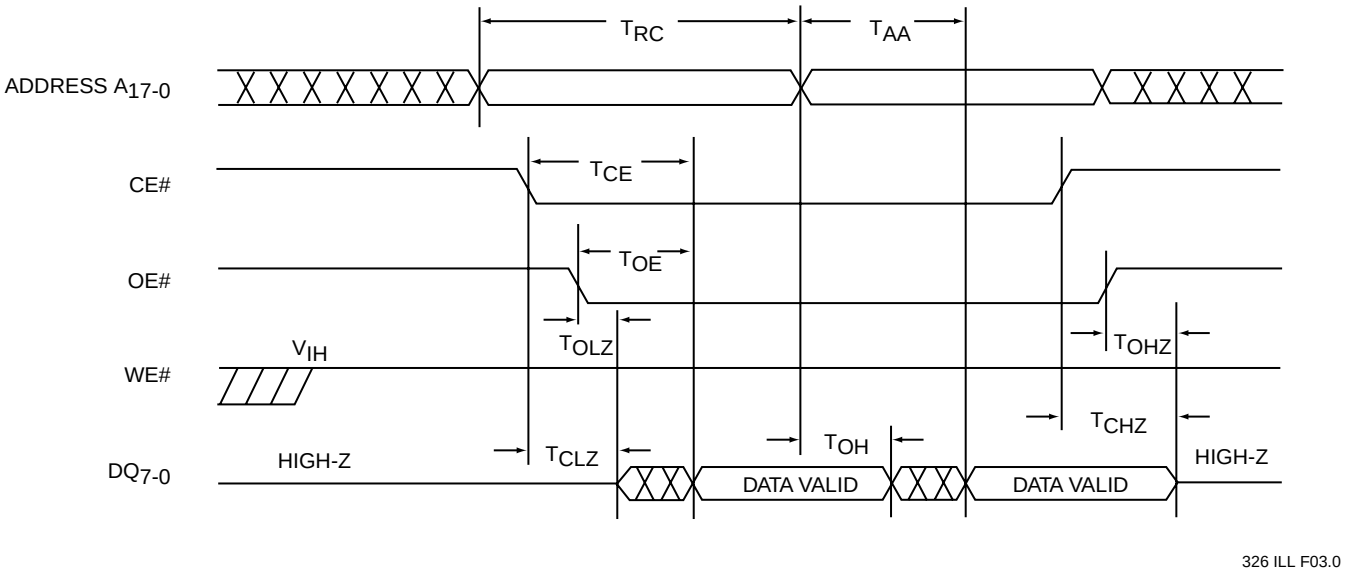


FIGURE 3: READ CYCLE TIMING DIAGRAM

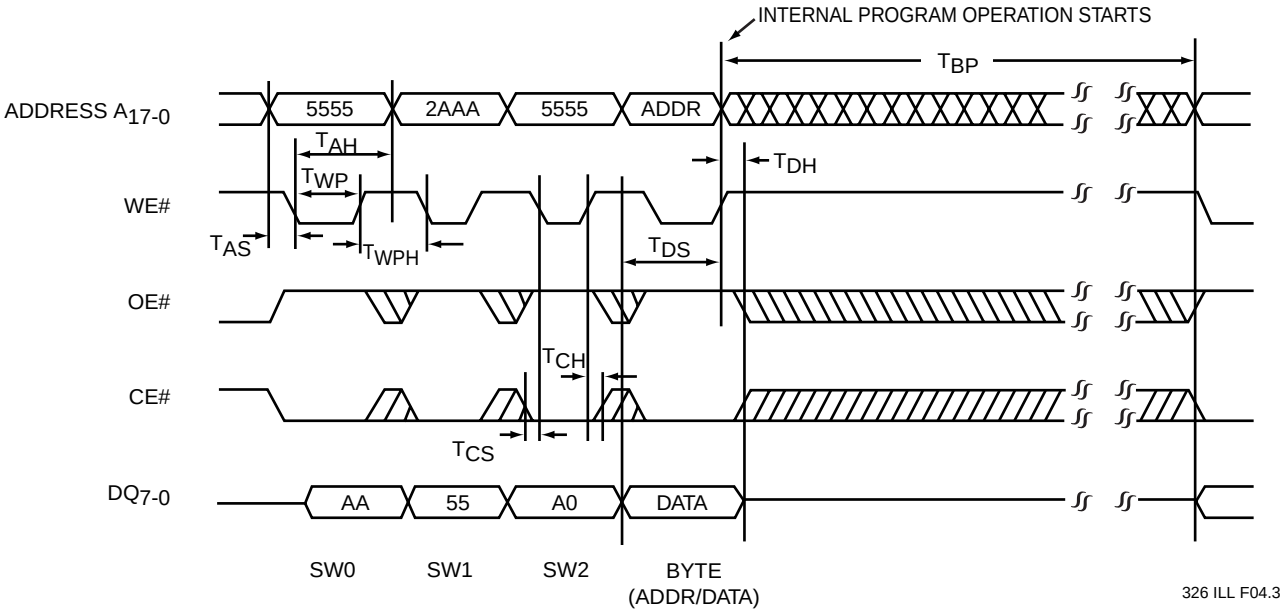


FIGURE 4: WE# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM

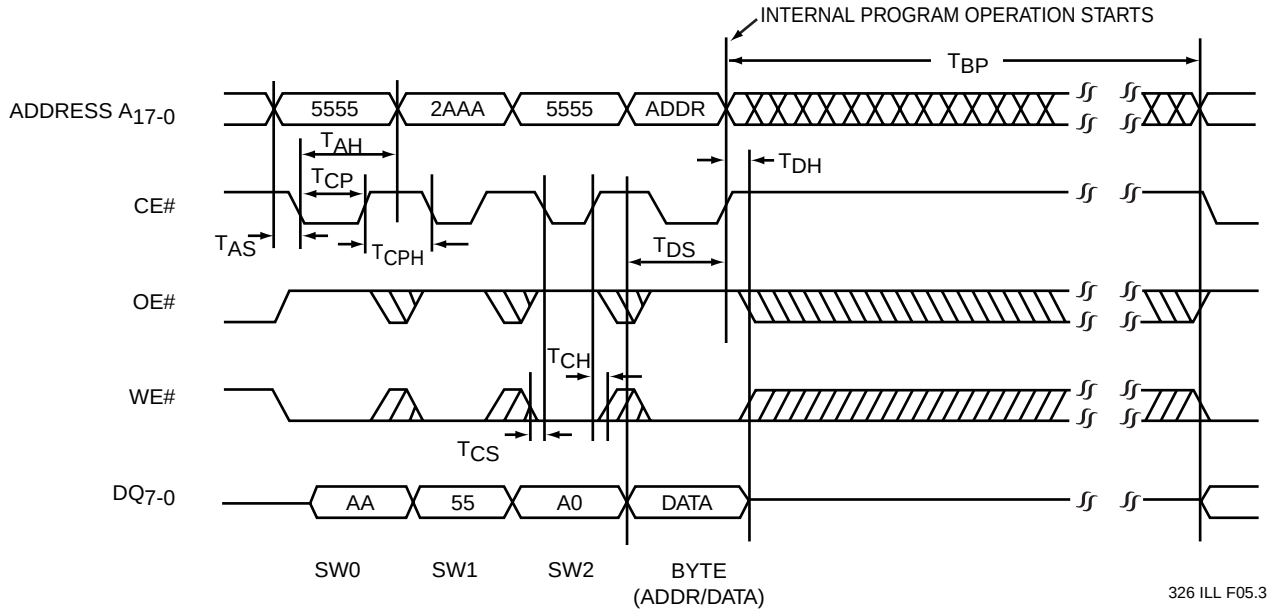


FIGURE 5: CE# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM

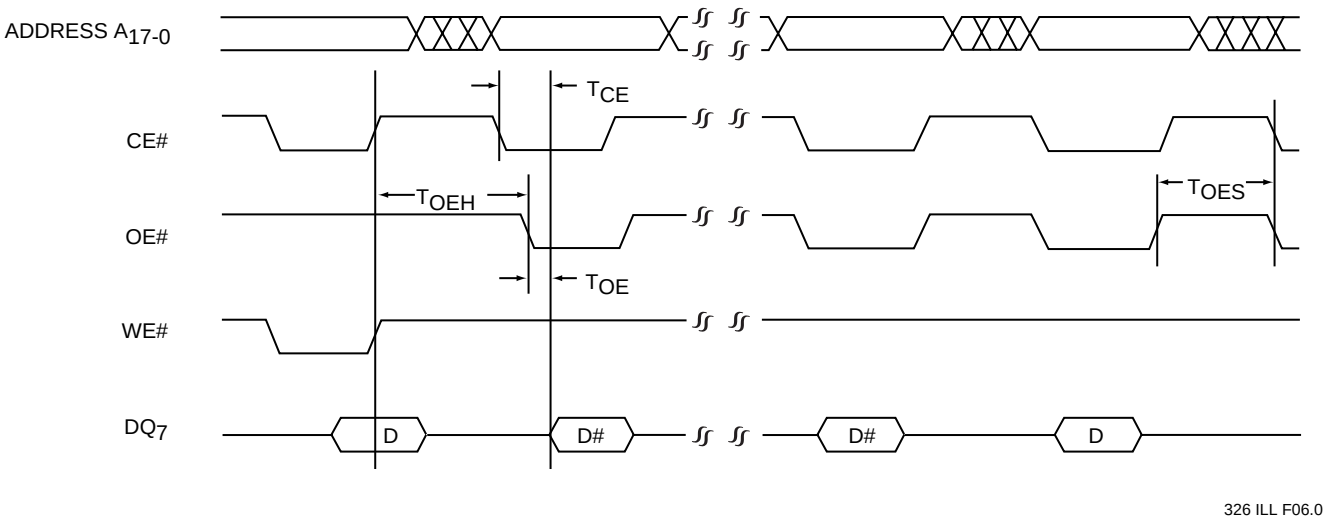


FIGURE 6: DATA# POLLING TIMING DIAGRAM

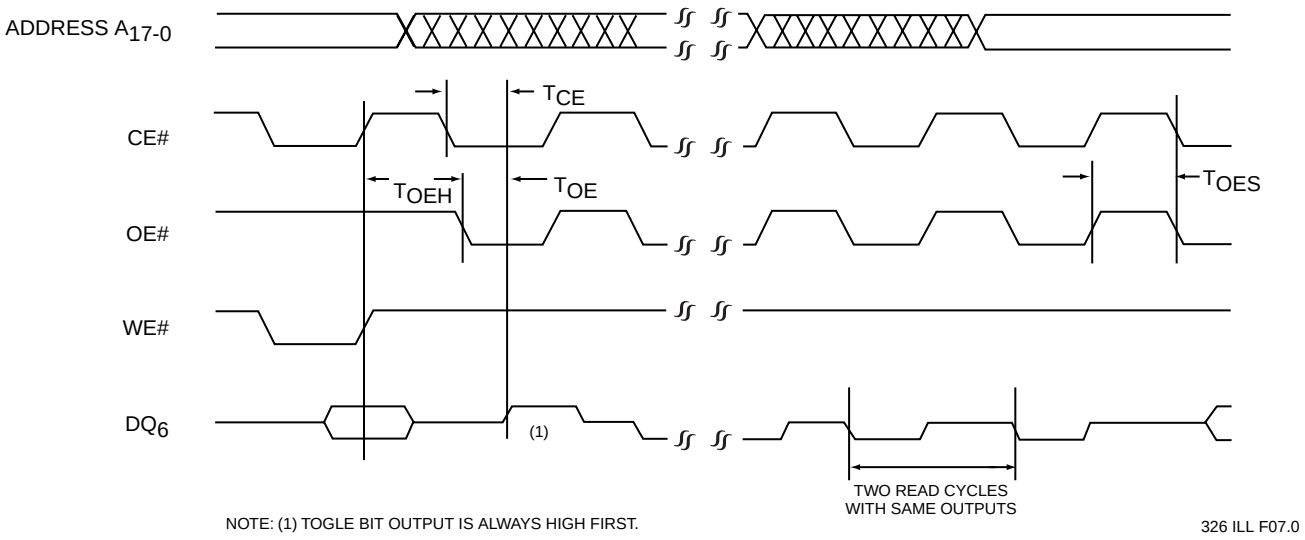
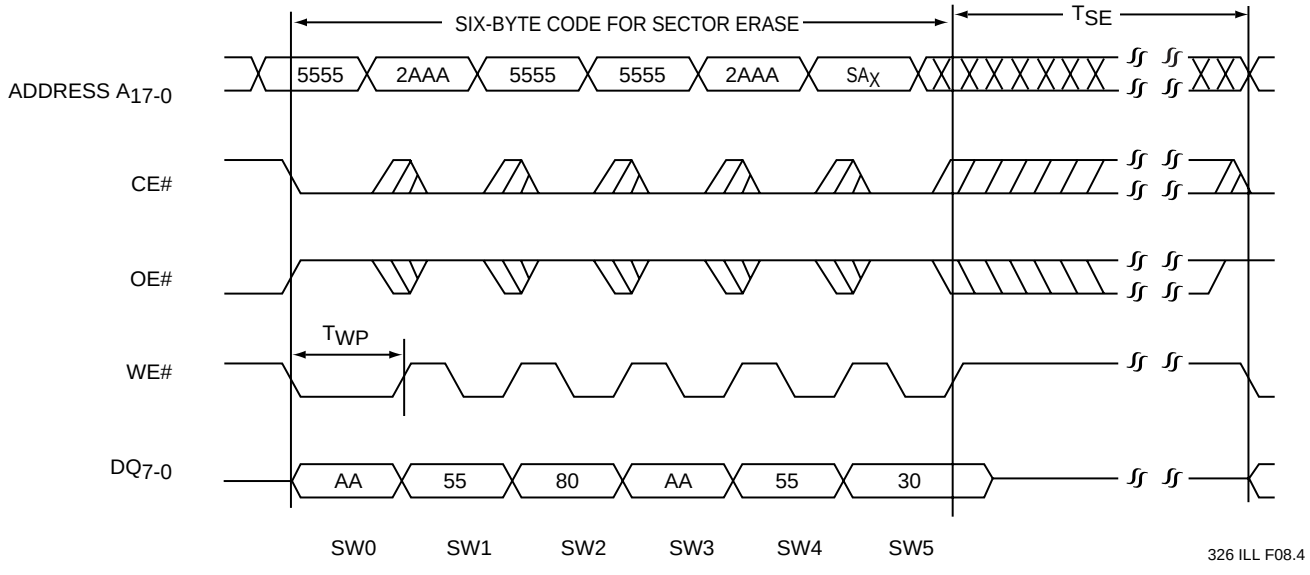
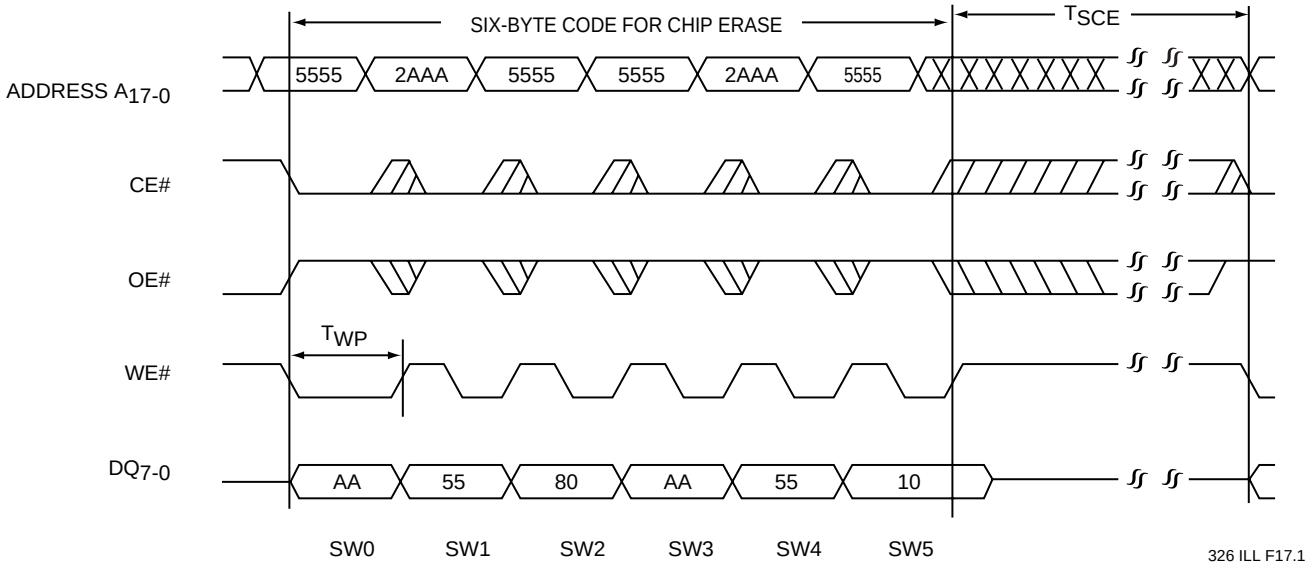


FIGURE 7: TOGGLE BIT TIMING DIAGRAM



Note: The device also supports CE# controlled sector erase operation. The WE# and CE# signals are interchangeable as long as minimum timings are met. (See Table 10)
SA_X = Sector Address

FIGURE 8: WE# CONTROLLED SECTOR ERASE TIMING DIAGRAM



Note: The device also supports CE# controlled chip erase operation. The WE# and CE# signals are interchangeable as long as minimum timings are met. (See Table 10)

FIGURE 9: WE# CONTROLLED CHIP ERASE TIMING DIAGRAM

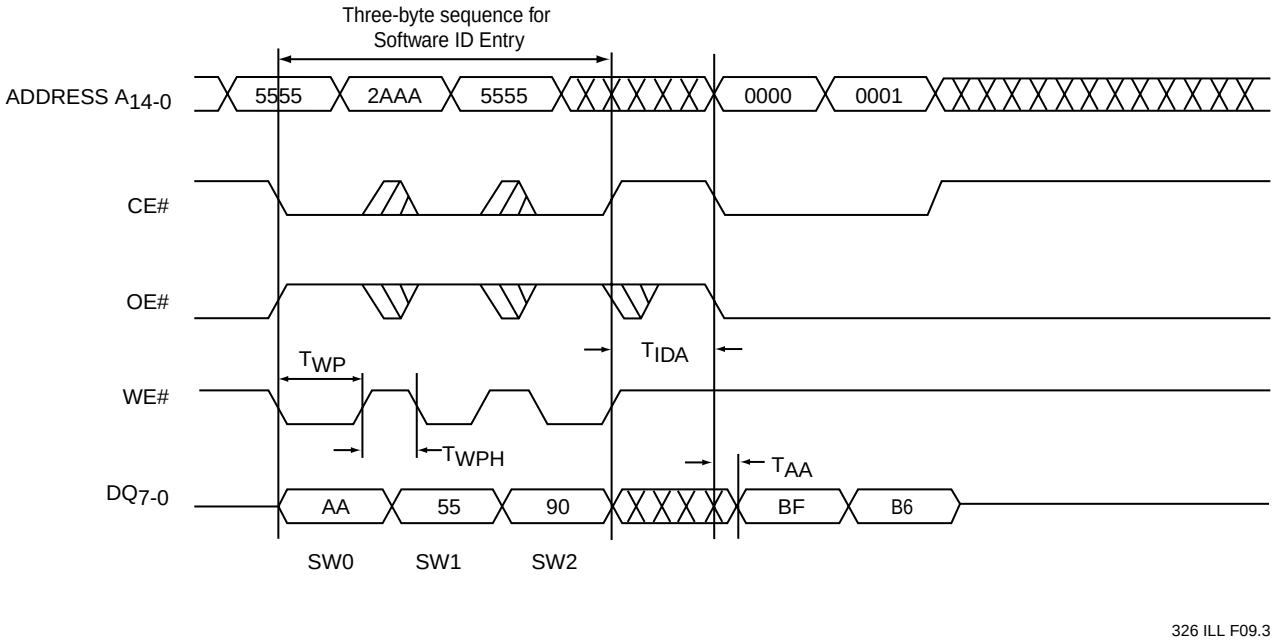


FIGURE 10: SOFTWARE ID ENTRY AND READ

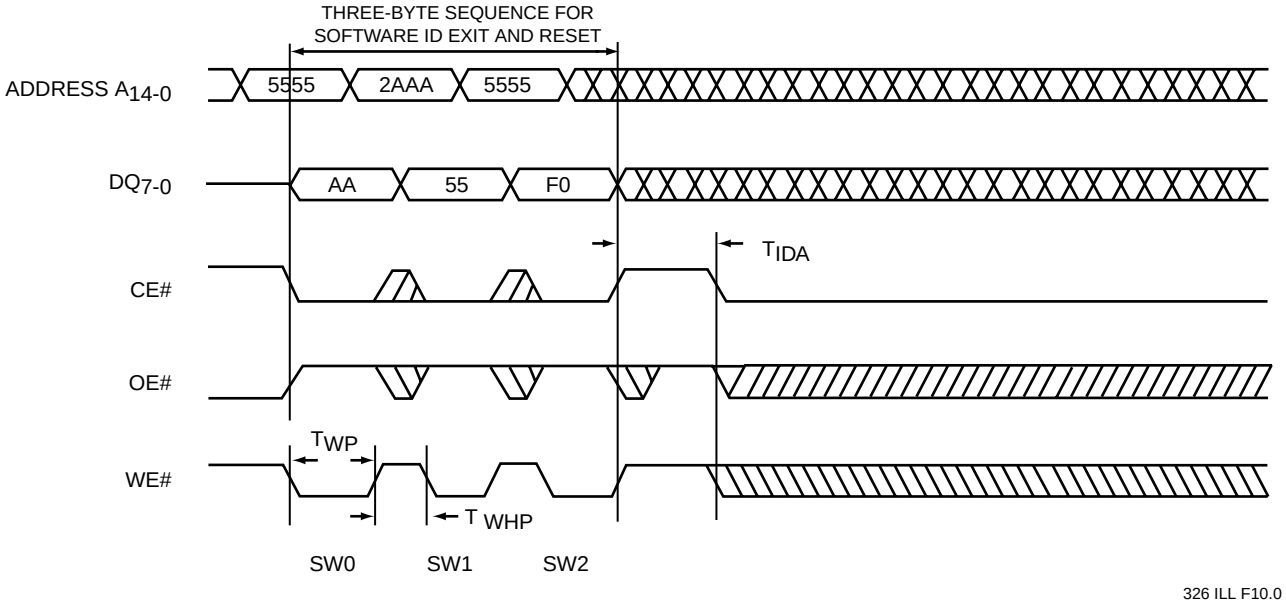
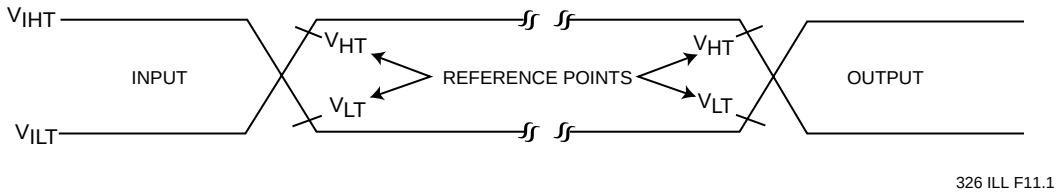


FIGURE 11: SOFTWARE ID EXIT AND RESET



AC test inputs are driven at V_{IHT} (2.4 V) for a logic “1” and V_{ILT} (0.4 V) for a logic “0”. Measurement reference points for inputs and outputs are V_{HT} (2.0 V) and V_{LT} (0.8 V). Inputs rise and fall times (10% ↔ 90%) are <10 ns.

Note: V_{HT}–V_{HIGH} Test
V_{LT}–V_{LOW} Test
V_{IHT}–V_{INPUT} HIGH Test
V_{ILT}–V_{INPUT} LOW Test

FIGURE 12: AC INPUT/OUTPUT REFERENCE WAVEFORMS

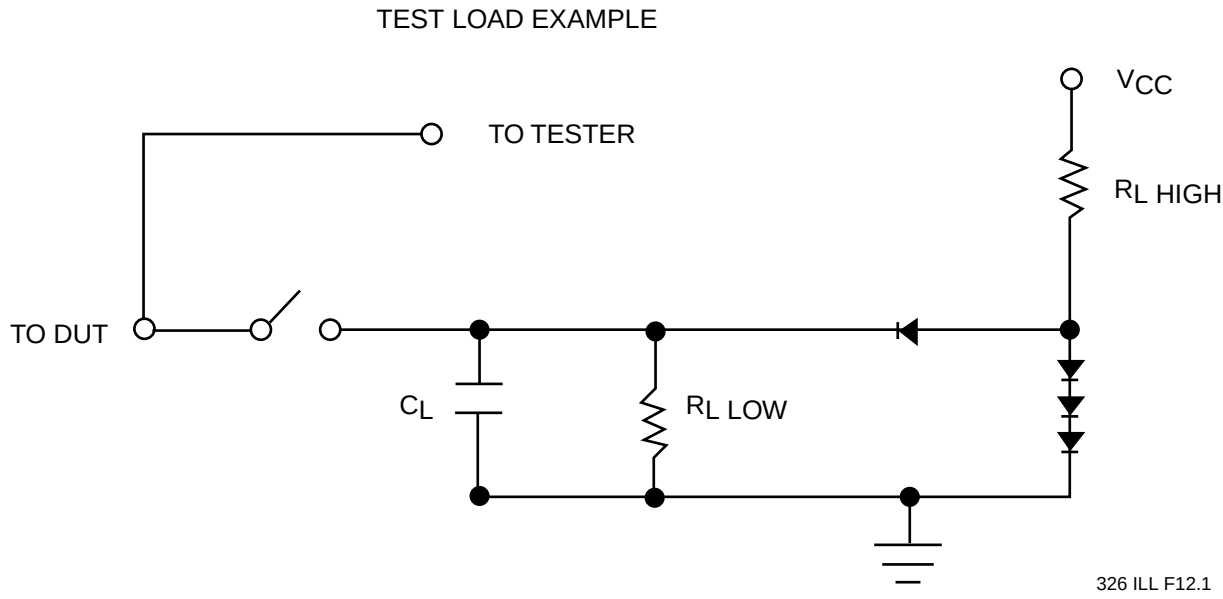


FIGURE 13: A TEST LOAD EXAMPLE

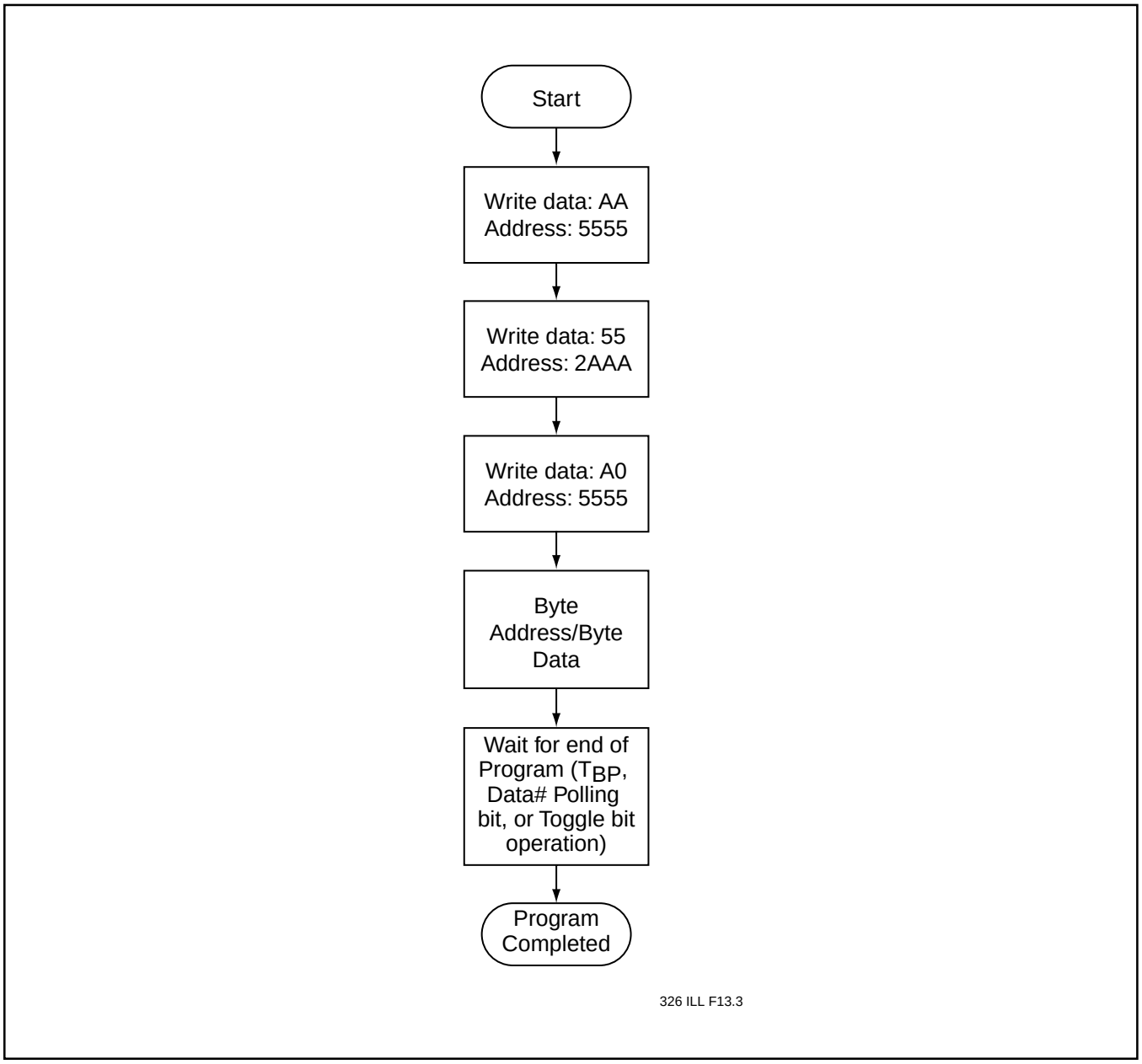


FIGURE 14: BYTE PROGRAM ALGORITHM

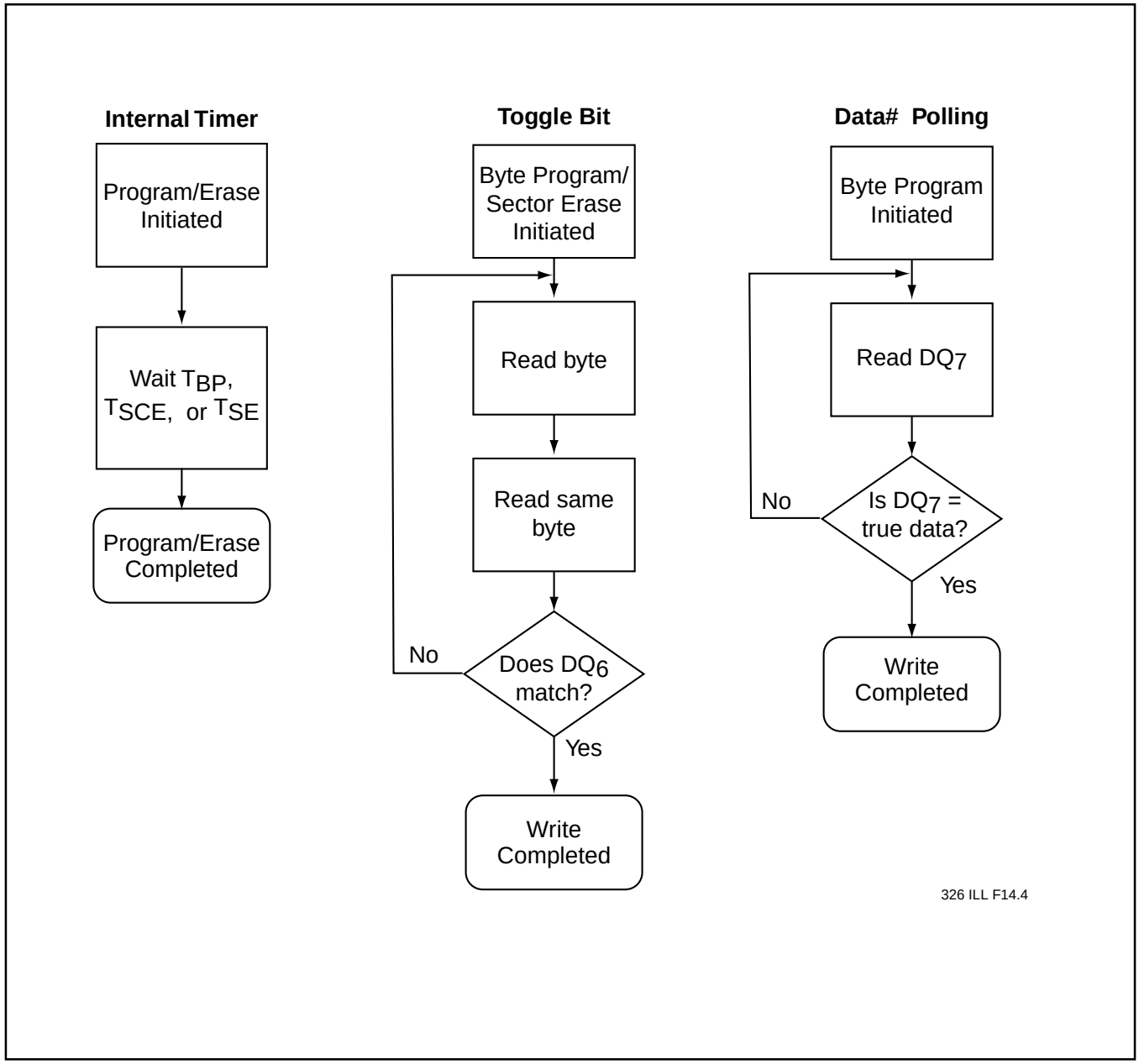


FIGURE 15: WAIT OPTIONS

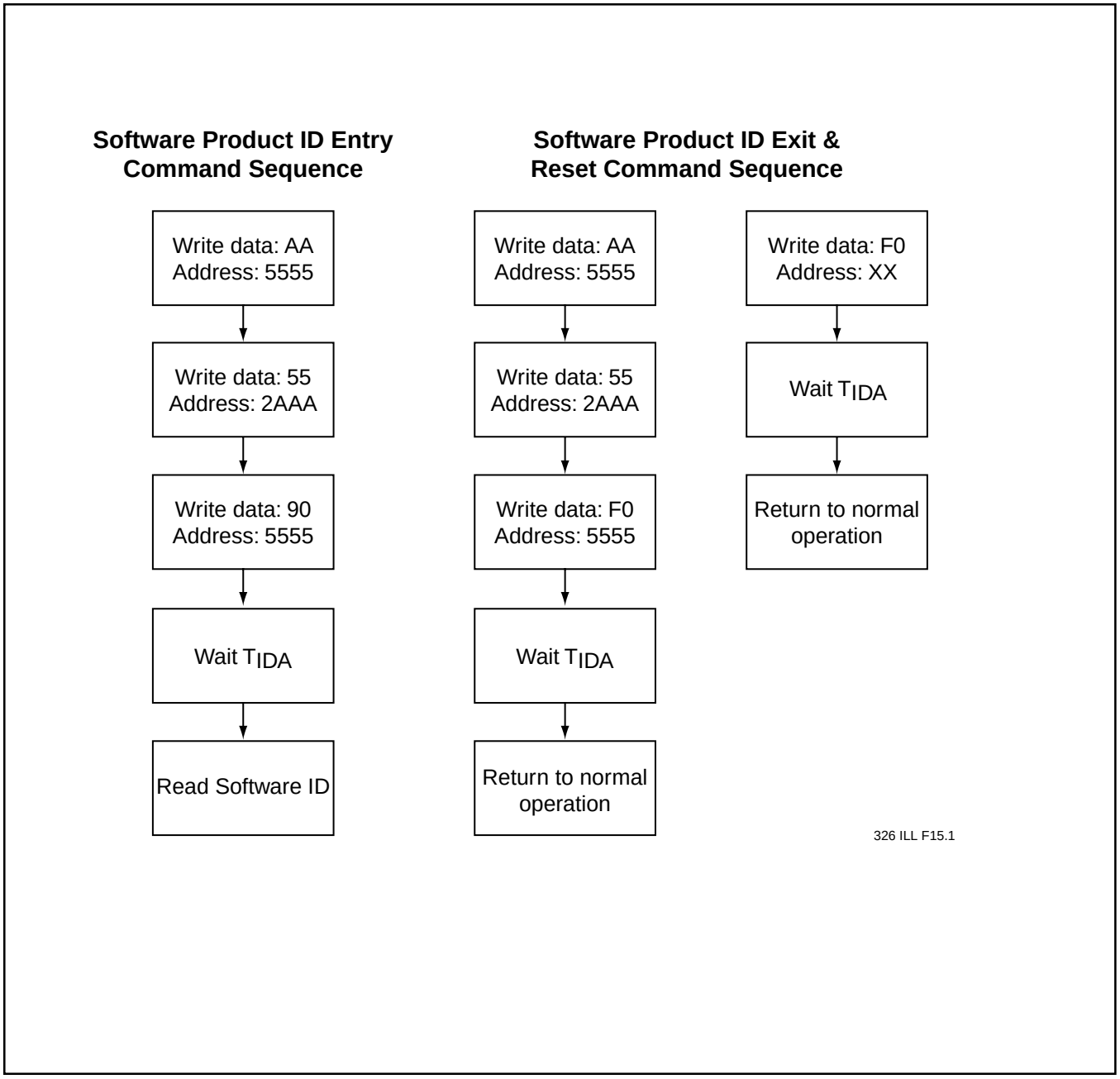


FIGURE 16: SOFTWARE PRODUCT COMMAND FLOWCHARTS

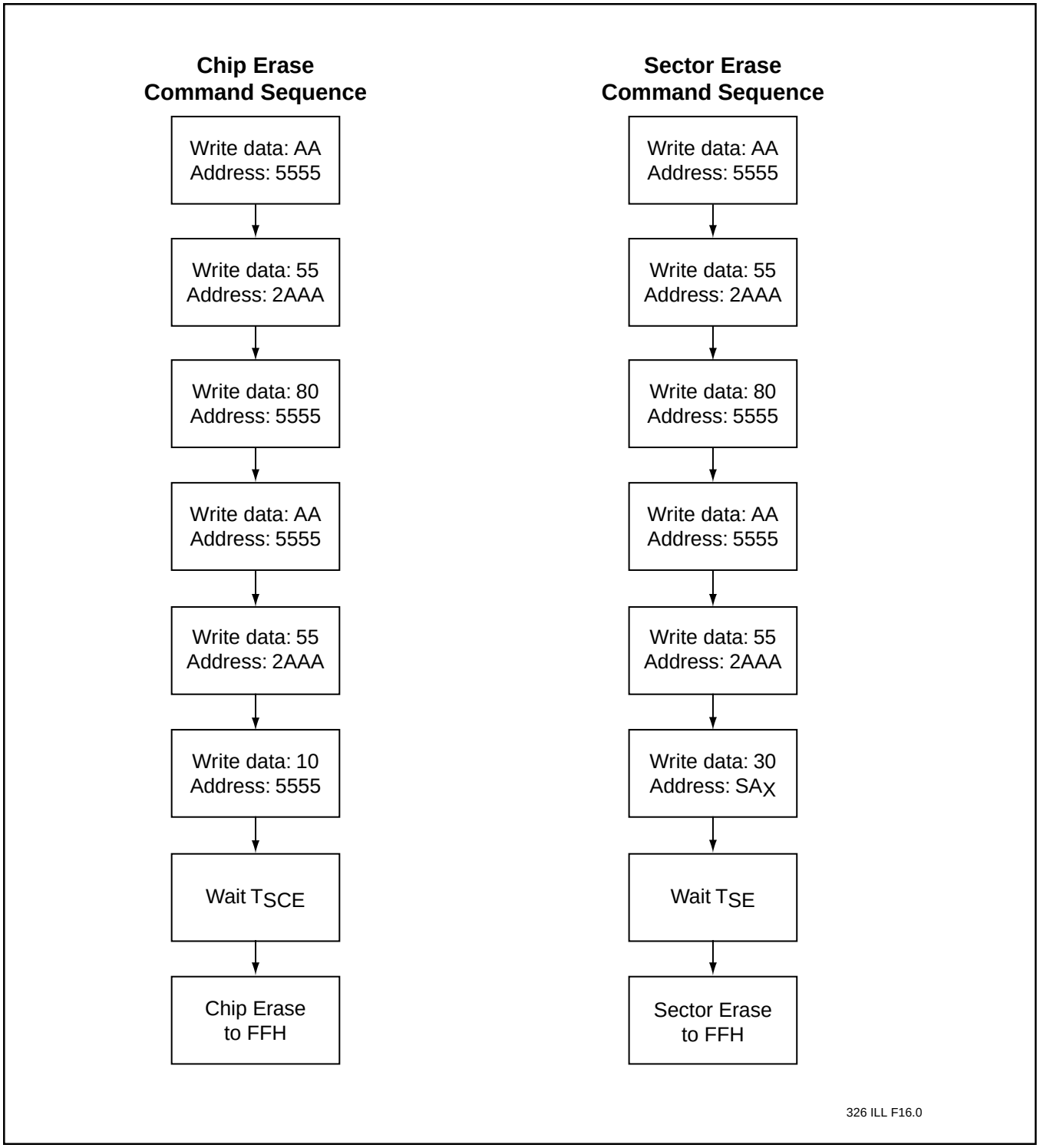
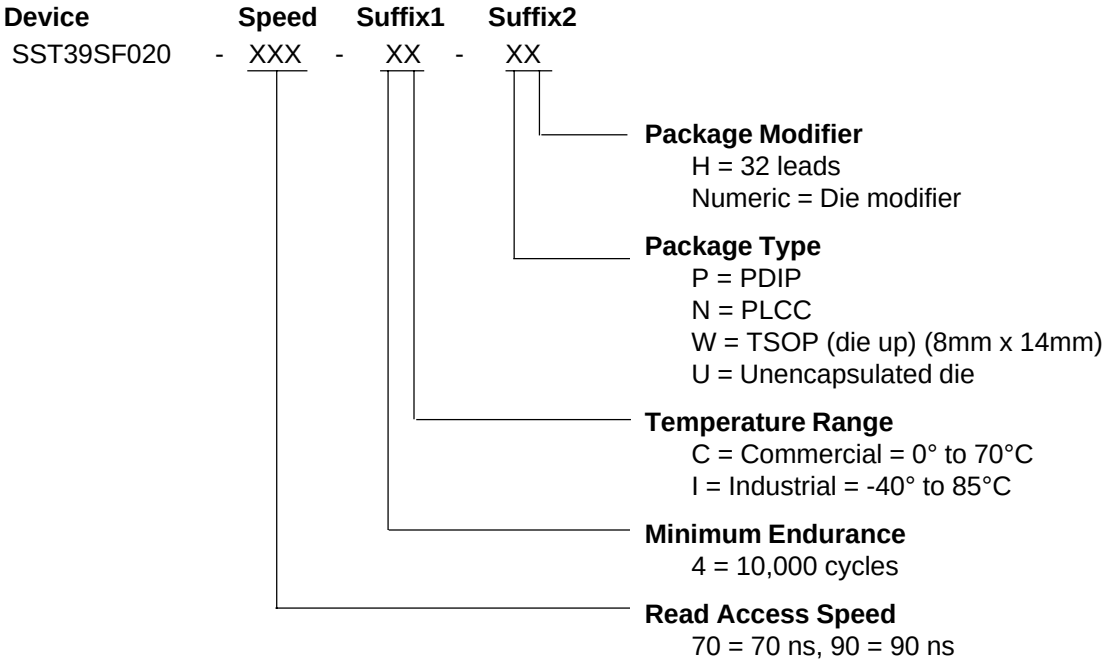


FIGURE 17: ERASE COMMAND SEQUENCE

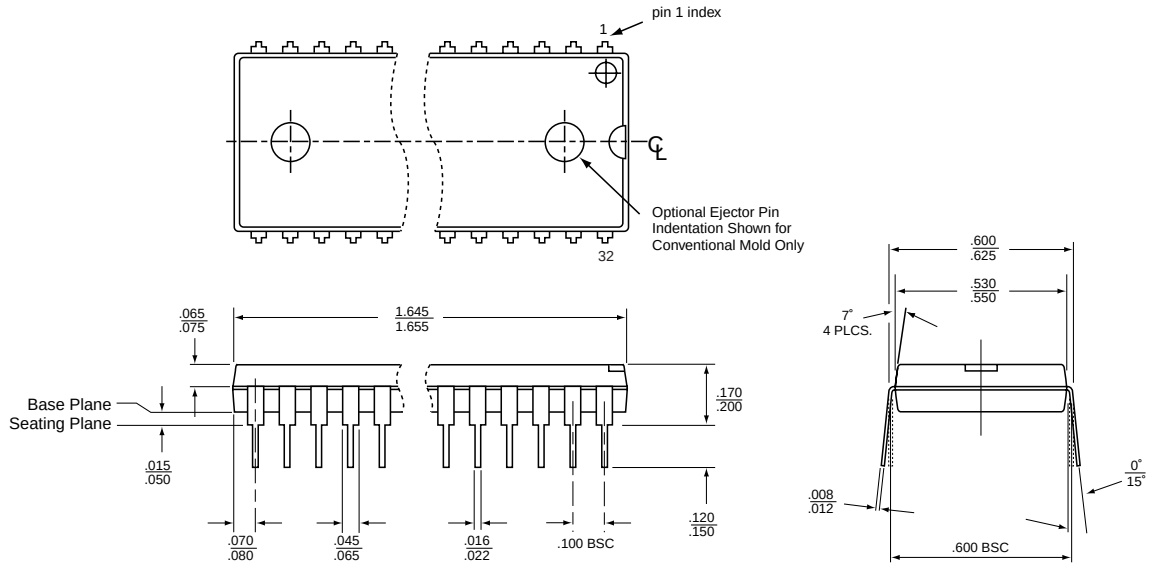


SST39SF020 Valid combinations

SST39SF020-70-4C-WH	SST39SF020-70-4C-NH	SST39SF020-70-4C-PH
SST39SF020-90-4C-WH	SST39SF020-90-4C-NH	SST39SF020-90-4C-PH
SST39SF020-90-4C-U1		
SST39SF020-70-4I-WH	SST39SF020-70-4I-NH	
SST39SF020-90-4I-WH	SST39SF020-90-4I-NH	

Example : Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

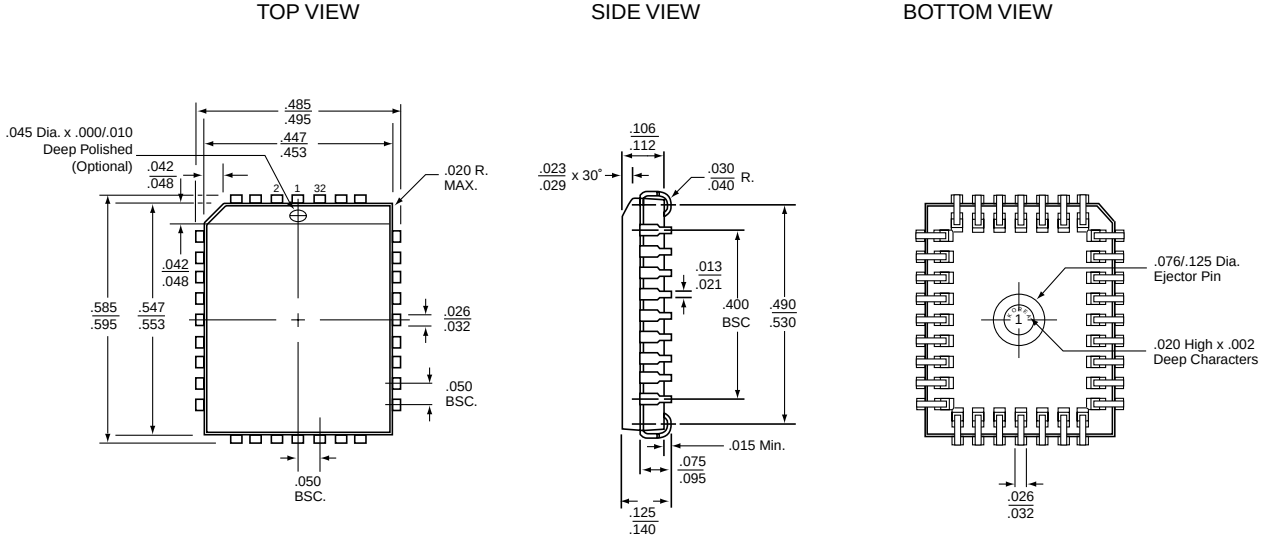
PACKAGING DIAGRAMS



Note: 1. Complies with JEDEC publication 95 MO-015 AP dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in inches (min/max).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .010 inches.

32.pdipPH-ILL.0

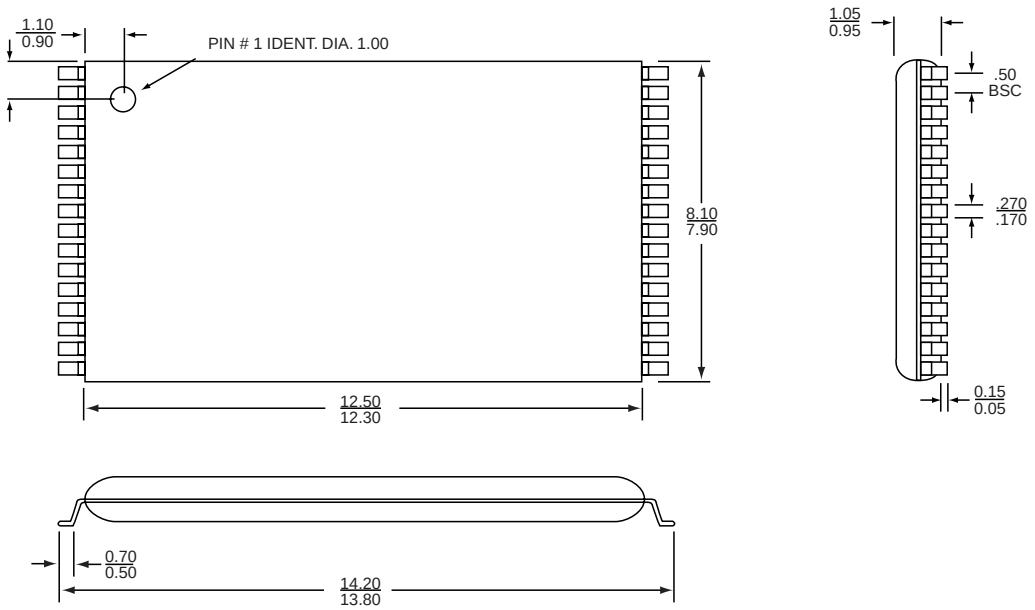
32-LEAD PLASTIC DUAL-IN-LINE PACKAGE (PDIP)
SST PACKAGE CODE: PH



Note: 1. Complies with JEDEC publication 95 MS-016 AE dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in inches (min/max).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .008 inches.

32.PLCC.NH-ILL.0

32-LEAD PLASTIC LEAD CHIP CARRIER (PLCC)
SST PACKAGE CODE: NH



Note: 1. Complies with JEDEC publication 95 MO-142 BA dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in metric (min/max).
3. Coplanarity: 0.1 (±.05) mm.

32.TSOP-WH-ILL.0

32-LEAD THIN SMALL OUTLINE PACKAGE (TSOP)
SST PACKAGE CODE: WH

NOTES: